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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,078	09/30/2003	Timothy V. Harper	200205879-3	8341

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)	
10/677,078	HARPER ET AL.	
Examiner	**Art Unit**	
Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-34* is/are pending in the application.

4a) Of the above claim(s) *26-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Newly submitted claims 26-34 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the original claims 13-25 are directed to a process of attaching a first integrated circuit die and a second integrated circuit die on a packing substrate. On the other hand, the new claims 26-34 are directed to a process of forming a stack of an integrated circuit by using a solder flux for attaching a second integrated circuit on a first integrated circuit before attaching the stack of the integrated circuit on a packing substrate.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 26-34 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Shimada (US. 6,365,963).

Shimada (Fig. 2) discloses a method of assembling an integrated circuit package Comprising: providing a package substrate 301 having a first surface including a first array of the interconnection sites 308 and a second array of interconnection sites 304; engaging a first integrated circuit die 303 with the package substrate 301 such that an array of interconnection sites 305 on a first surface of the first integrated circuit die 303 are substantially aligned with the second array of the interconnection sites 304 of the package substrate 301; electrically connecting the second array of the interconnection sites 304 to the array of interconnection sites 305 of the first integrated circuit die 303; engaging a second integrated circuit die 307 with the package substrate 301 such that an array of the interconnection sites 309 on a first surface of the second integrated circuit die 307 are substantially aligned with the first array of the interconnection sites 308 of the package substrate, with the first integrated circuit die 303 positioned amid the package substrate 301 and the second integrated circuit die 307; and electrically connecting the first array of the interconnection sites 308 to the array of the interconnection sites 309 of the second integrated circuit die 307, wherein at least one array of the interconnection sites 311 that is concentric with the first and second arrays of interconnection sites 304/308 remains uncovered by the first and second integrated circuits 303/307.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13-15 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada (US. 6,365,963) in view of Kelkar et al (US. 6,084,308).

Regarding claims 13, 15 and 21-22, as discussed in details above, Shimada's Fig. 2 substantially reads on the above claims, except it does not specifically disclose that the connection of the first array of the interconnection sites 308 to the array of the interconnection sites 309 of the second integrated circuit die 307, and the second array of the interconnection sites 304 to the array of the interconnection sites 305 of the first integrated circuit die 303 are performed by simultaneous reflowing solder.

However, Kelkar (Figs. 4A and 5) teaches a method of assembling an integrated circuit package by: first attaching the die stack of the first die 306 and the second die 316 over the package substrate 302; and then simultaneously reflowing solder between the first array of interconnection sites of the package substrate and the array of interconnection sites of the second integrated circuit die 316, and between the second array of interconnection sites of the package substrate and the array of interconnection sites of the first integrated circuit die 306 (also see column 8, lines 16-23). Accordingly, it would have been obvious to connect the first die 303 and the second die 307 of Shimada to the package substrate by performing a single reflow process when the array of solder bumps of the first integrated circuit die and the array of solder bumps of the second integrated circuit die have a substantially a same reflow temperature, as taught by Kelkar (column 3, lines 24-32).

Regarding claim 14, Shimada's Fig. 2 further discloses the package substrate 301 defines a recessed area 302 that includes the second array of interconnection sites 304 and wherein the step of engaging the first integrated circuit die 303 with the package substrate 301 includes: positioning the first integrated circuit die 303 within the recessed area of the package substrate 301.

6. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al (US. 6,489,686) in view of Kelkar et al (US. 6,084,308) and Bertin et al (US. 5,977,640).

Regarding claims 13-15 and 20-22, Farooq (Fig. 1) discloses a method of assembling an integrated circuit package comprising: providing a package substrate 50 having a first surface including a first array of interconnection sites and a second array of interconnection sites 42; engaging a first integrated circuit die 10 with the package substrate 50 such that an array of interconnection sites on a first surface of the first integrated circuit die 10 are substantially aligned with the second array of interconnection sites of the package substrate 50; engaging a second integrated circuit die 20 with the package substrate 50 such that an array of interconnection sites on a first surface of the second integrated circuit die 20 are substantially aligned with the first array of interconnection sites of the package substrate 50, with the first integrated circuit die 10 positioned within the recessed area of the package substrate 50 and amid the package substrate 50 and the second integrated circuit die 20; and electrically connecting the first array of interconnection sites 42 to the array of interconnection sites of the second integrated circuit die 20, and the second array of interconnection sites 42 to the array of interconnection sites of the first integrated circuit die 10 (column 4, lines 56-65).

Farooq does not disclose that the connection of the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die 20 and the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die 10 are performed by simultaneously reflowing solder.

However, Kelkar (Figs. 4A and 5) teaches a method of assembling an integrated circuit package by: first attaching the die stack of the first die 306 and the second die 316 over the package substrate 302; and then simultaneously reflowing solder between the first array of interconnection sites of the package substrate and the array of interconnection sites of the second integrated circuit die 316, and between the second array of interconnection sites of the package substrate and the array of interconnection sites of the first integrated circuit die 306 (also see column 8, lines 16-23). Accordingly, it would have been obvious to fabricate a chip-on-chip package of Farooq by performing the connections of the first die and the second die to the package substrate with the processes as set forth above because as taught by Kelkar, such processes would allow the combined first and second dies to be moved by placement equipment without the dies coming apart before they are placed on and simultaneously attached to the package substrate (column 8, lines 2-11).

Neither Farooq nor Kelkar disclose one array of interconnection sites located on the first surface of the substrate remains uncovered by the first and second integrated circuits.

However, Bertin (Fig. 14) teaches the forming of an array of interconnection sites 82/84 located on the first surface of the substrate and remaining uncovered by the first and second integrated circuits 30/40. Accordingly, it would have been obvious to further form the array of the interconnection sites located on the first surface of the substrate with the structure as set forth above in order to provide the electrical connections to the external devices, as taught by Bertin (column 5, lines 33-36).

Regarding claims 16-18 and 23-25, Kelkar (Figs. 4A and 5) further teaches the process step of aligning a further array of interconnection sites on the first surface of the second integrated circuit die 316 with an additional array of interconnection sites on a second surface of the first integrated circuit die 306, and the process step of simultaneously reflowing solder (a first reflow process) between the further array of interconnection sites of the second integrated circuit die 316 and the additional array of interconnection sites on the second surface of the first integrated circuit die 306 (see column 8, lines 1-8).

Regarding claim 19, Kelkar (step 508 of Fig. 5) further teaches the step of simultaneously reflowing solder (a second reflow process) between the second array of interconnection sites and the array of interconnection sites of the first integrated circuit die 306, between the first array of interconnection sites and the array of interconnection sites of the second integrated circuit die 316, and between the further array of interconnection sites of the second integrated circuit 316 and the additional array of interconnection sites on the second surface of the first integrated circuit die 306 (see column 8, lines 16-24).

7. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick (US. 6,369,448) in view of Kelkar et al (US. 6,084,308) and Bertin et al (US. 5,977,640).

Regarding claims 13, 15, and 20-22, McCormick (Fig. 4) discloses a method of Assembling an integrated circuit package comprising: providing a package substrate 402 having a first surface including a first array of interconnection sites 414 and a second array of interconnection sites 416; engaging a first integrated circuit die 412 with the package substrate 402 such that an array of interconnection sites on a first surface of the first integrated circuit die 412 are substantially aligned with the second array of interconnection sites 416 of the package substrate 402; engaging a second integrated circuit die 410 with the package substrate 402 such that an array of interconnection sites on a first surface of the second integrated circuit die 410 are substantially aligned with the first array of the interconnection sites 414 of the package substrate 402, with the first integrated circuit die 412 positioned amid the package substrate 402 and the second integrated circuit die 410; and electrically connecting the first array of interconnection sites 414 to the array of interconnection sites of the second integrated circuit die 410, and the second array of interconnection sites 416 to the array of interconnection sites of the first integrated circuit die 412 (column 7, lines 15-37).

McCormick does not disclose that the connection of he first array of interconnection sites 414 to the array of interconnection sites of the second integrated circuit die 410 and the second array of interconnection sites 416 to the array of interconnection sites of the first integrated circuit 412 are performed by simultaneously reflowing solder.

However, Kelkar (Figs. 4A and 5) teaches a method of assembling an integrated circuit package by: first attaching the die stack of the first die 306 and the second die 316 over the package substrate 302; and then simultaneously reflowing solder between the first array of interconnection sites of the package substrate and the array of interconnection sites of the second integrated circuit die 316, and between the second array of interconnection sites of the package substrate and the array of interconnection sites of the first integrated circuit die 306 (also see column 8, lines 16-23). Accordingly, it would have been obvious to fabricate a chip-on-chip package of McCormick by performing the connections of the first die and the second die to the package substrate with the processes as set forth above because as taught by Kelkar, such processes would allow the combined first and second dies to be moved by placement equipment without the dies coming apart before they are placed on and simultaneously attached to the package substrate (column 8, lines 2-11).

Neither McCormick nor Kelkar disclose one array of interconnection sites located on the first surface of the substrate remains uncovered by the first and second integrated circuits.

However, Bertin (Fig. 14) teaches the forming of an array of interconnection sites 82/84 located on the first surface of the substrate and remaining uncovered by the first and second integrated circuits 30/40. Accordingly, it would have been obvious to further form the array of the interconnection sites located on the first surface of the substrate with the structure as set forth above in order to provide the electrical connections to the external devices, as taught by Bertin (column 5, lines 33-36).

Regarding claims 16-18 and 23-25, Kelkar (Figs. 4A and 5) further teaches the process step of aligning a further array of interconnection sites on the first surface of the second integrated circuit die 316 with an additional array of interconnection sites on a second surface of the first integrated circuit die 306, and the process step of simultaneously reflowing solder (a first reflow process) between the further array of interconnection sites of the second integrated circuit die 316 and the additional array of interconnection sites on the second surface of the first integrated circuit die 306 (see column 8, lines 1-8).

Regarding claim 19, Kelkar (step 508 of Fig. 5) further teaches the step of simultaneously reflowing solder (a second reflow process) between the second array of interconnection sites and the array of interconnection sites of the first integrated circuit die 306, between the first array of interconnection sites and the array of interconnection sites of the second integrated circuit die 316, and between the further array of interconnection sites of the second integrated circuit 316 and the additional array of interconnection sites on the second surface of the first integrated circuit die 306 (see column 8, lines 16-24).

Regarding claim 14, Kelkar (Fig. 4A) further teaches the step of positioning the first integrated circuit die 306 within the recesses area of the package substrate 302 for providing a relatively small overall package size and high reliability (column 2, lines 45-50).

Response to Arguments

8. Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection. Because of the new issues presented in the amended claims, the new references are applied in the new ground of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
August 5, 2004

PHAT X. CAO
PRIMARY EXAMINER